TITLE: **BACK-TO-BACK CONNECTED POWER SEMICONDUCTOR DEVICE PACKAGE**

RELATED APPLICATION

[0001] This application claims the benefit of U.S. Provisional Application No. 60/262,890, filed January 19, 2001.

FIELD OF THE INVENTION

[0002] This invention relates to semiconductor device packages and more specifically relates to a novel package having a minimized area or "footprint".

BACKGROUND OF THE INVENTION

[0003] Many packages are known which contain plural semiconductor die such as two power MOSFETs, or other switching or MOSgated devices (MOSFETs, IGBTs, thyristors, and the like) or a power MOSgated device die and a control circuit die for the power MOSFET die. Such packages can define series or parallel connected die or a "smart" power semiconductor in which a power device is controlled by an integrated circuit die. These die are generally laid out side by side and are laterally spaced atop a lead frame, or other support surface and are connected through the lead frame and/or by wire bonds to their upper surfaces. Other geometries are known in which one chip is fixed to the top of another chip, with the chips interconnected by laterally displaced wire bonds to a lead frame.

[0004] These arrangements of die take up lateral space or area and a relatively large "footprint" or area is required on the support substrate to support the die.

[0005] In applications, in which space is at a premium, as in portable electronic devices, it would be desirable to provide a package structure which could have the same effective active area of silicon for the power die and control die but which has a reduced footprint on the support such as a printed circuit board.

BRIEF DESCRIPTION OF THE INVENTION

[0006] In accordance with the invention, first and second semiconductor die are mounted on the opposite respective surfaces of a copper (or other conductive material) lead frame mounting pad, in lateral alignment with one another. The two die may be identical MOSgated devices such as MOSFETs or IGBTs, with their drain electrodes connected to the opposite lead frame surfaces by a suitable die attach material such as a silver loaded epoxy adhesive. The source and gate leads may then be wire bonded to lead frame pins and the die and lead frame can then be overmolded with a plastic mold. The device may, for example, define a bidirectional switch structure with a common drain.

[0007] Alternatively, the package may contain one (or more) power die on one side of the lead frame mounting pad and a control IC therefore on the other side of the lead frame pad. In this case, the IC may be electrically isolated from the lead frame, using an insulation polyimide film or an insulation die attach adhesive.

[0008] The die attach process may involve two stages, one for each die. Each stage involves an adhesive dispense step, a die placement step and a cure step for each die. Alternatively, an adhesive with a suitable uncured adhesive strength which can hold the die in place can be used to temporarily hold the die in place on the lead frame and the two die adhesive bonds may be cured simultaneously.

[0009] Note that one or more of the die may be thinned prior to die bonding to minimize package height.

[0010] After both die are bonded to the lead frame, electrical connection to the lead frame pins is made, using either wire bonding or a copper strap technology. In the case of wire bonding, very low resistance material, such as gold or aluminum is preferably used.

[0011] Once the electrical connections are completed between both die and lead frame pins, the assembly is encapsulated in mold compound in the well known manner. The whole assembly is then cured at a high curing temperature. Each device assembly is then separated from the lead frame using typical trim and singulation stages. The singulated devices are then tested and laser marked as usual for semiconductor device packages.

[0012] The novel package of the invention is useful where:

[•] Low R_{DSON} devices are required;

[•] Space is at a premium (i.e. in portable hand held applications);

[•] Where "smart" switching (FET plus control IC) is required with a small footprint;

[0013] Where MOSFETs with a common drain topology are required, as in battery protection circuit.

[0014] The present invention provides the benefit of doubling device active area for a given package area, compared with standard surface mounted transistor devices; and can provide smart power MOSFET devices without compromising MOSFET active area for a given footprint area.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] Figure 1 is a top view of a lead frame segment with a top die in place and wire bonded to the lead frame pins.

[0016] Figure 2 is a cross-section of Figure 1 taken across section line 2-2 in Figure 1 and shows both top and bottom power MOSFET die connected to the top and bottom surfaces of a common lead frame pad.

[0017] Figure 3 is a top view of the singulated package of Figure 2 and shows the output pin out pattern of the package.

[0018] Figure 4 is a circuit diagram of the device of Figures 1 to 3.

[0019] Figure 5 is a cross-section of a second embodiment of the invention in which a single power MOSgated device and an integrated control circuit die therefor are mounted on opposite surfaces of a single lead frame pad.

[0020] Figure 6 is a circuit diagram of the device of Figure 5.

[0021] Figure 7 is a top view of the package of the device of Figures 5 and 6.

DETAILED DESCRIPTION OF EMBODIMENTS OF THE INVENTION

[0022] Referring first to Figure 1, there is shown a conventional lead frame 20 which is a thin conductive stamping of copper or a copper alloy or the like which has a plurality of identical segments, one of which is shown. The segment shown has an enlarged die-receiving pad 21 and a plurality of lead pins 22 to 29, 4 pins on each side of the pad 21 to define an 8 pin in-line package. Other numbers of pins and different package pin-out topologies can also be used with the invention.

Sub a1> **[0023]** In accordance with the invention, and as shown in Figures 1 and 2, the drain electrodes of two power MOSFET die 30 and 31 are conductively fixed to the opposite top and bottom surfaces of the lead frame 21. Thus, they can be connected by conductive adhesive layers such as layers 32 and 33 respectively in

Figure 2. Layers 32 and 33 may be epoxies with silver particles loaded therein. Solder and tape can also be used. The first and second die are bonded so that they will not release from the lead frame during solder reflow. This arrangement connects the drains of each of MOSFETs 30 and 31 to a common drain node D (pad 21) as shown in Figure 4.

[0024] The source electrodes on the opposite surfaces of MOSFETs 30 and 31 and the gate electrodes on the same surfaces are then wire bonded to selected ones of the lead frame pins. Thus, sets of wire bonds connect the source electrode of die 30 to pins 22 and 23 while the gate electrode of die 30 is wire-bonded to pin 26.

[0025] The bottom die 31 is similarly wire-bonded to other pins and, for example, its source electrode can be wire-bonded to pins 24 and 25 and its gate wire-bonded to pin 29. The sources of die 30 and 31 may also be bonded to pins 27 and 28 respectively so that the gate pin for each MOSFET is adjacent a respective source (Kelvin) pin.

[0026] The various electrodes of die 30 and 31 can be connected to different pins, as desired and the pins can be internally connected within the package. Further, die 30 and 31 could be IGBT or thyristor die or diodes if desired, and different combinations of such die, for example, one IGBT die and a series connected diode die could be used.

[0027] After wire bonding, the lead frame is overmolded with suitable plastic housing, shown as housing 40 (in dotted lines in Figure 1 and in solid line in Figures 2 and 3.

[0028] Since die 30 and 31 are arranged atop one another (in spacial overlapping relation), the area they occupy in the package is reduced.

[0029] The resulting circuit shown in Figure 4 is a common drain bidirectional switching device which is very useful in numerous applications such as

for battery protection and the like. Further, the resulting package has a relatively small footprint as is very desirable for portable electronic applications such as cellular telephones and other hand held or portable devices such as pocket organizers and lap-top computers.

[0030] Figures 5, 6 and 7 show another embodiment of the invention in which power semiconductor device 30 is copacked with a control integrated circuit (IC) die 50 which controls device 30 and can act to turn device 30 on and off in response to such parameters as temperature (of die 30), current, over and undervoltages, rate of current and the like. Thus, the overall device becomes a "smart" MOSgated device.

sub a2

[0031] In Figures 5, 6 and 7, parts identical to these of Figures 1 to 4 have the same identifying numeral. The IC die 50 is connected to the bottom of pad 21 by an insulation adhesive 51 (Figure 5) such as a polyimide or the like. The IC can derive its operating power from leads 23 and 27 and has a control input terminal connected to pin 26 and an output line 52 which is internally wire bonded to the gate electrode of die 30. The source electrode of die 30 may be wire bonded to one or more of pins 22 to 25.

[0032] The final device package 40 has the same reduced "footprint" as that of Figures 1 to 4 and thus desirable for use in portable electronics.

[0033] It should be further noted that the package 40 will have a small height. The die 30 and 31 can be back-ground down to be as thin as possible to reduce this height.

[0034] In a still further embodiment of the invention, a buck converter circuit can be produced in which the top die 30 of Figure 2 would be an N channel synchronous MOSFET and the bottom die 31 a P channel control MOSFET. Any number of other circuits with mixed MOSgated devices could be employed.

[0035] Although the present invention has been described in relation to particular embodiments thereof, many other variations and modifications and other uses will become apparent to those skilled in the art. It is preferred, therefore, that the present invention be limited not by the specific disclosure herein, but only by the appended claims.